1. Philosophy of Reliability Monitoring

In order to guarantee the high standard of reliability for each product family, a reliability monitoring methodology linked with MTR (electronic-Manufacturing Trouble Report) system is executed. By monitoring the data of post burn-in yield, RAE department will determine if sampling burn-in is needed for any specified lots. To screen out any potential failure parts, it is necessary to do 100% re-burn-in for the whole mother lot if the sampling burn in result is substandard. The reliability monitoring process flow is shown in below Figure 1.

ISSI Memory Product
Process Monitor Plan

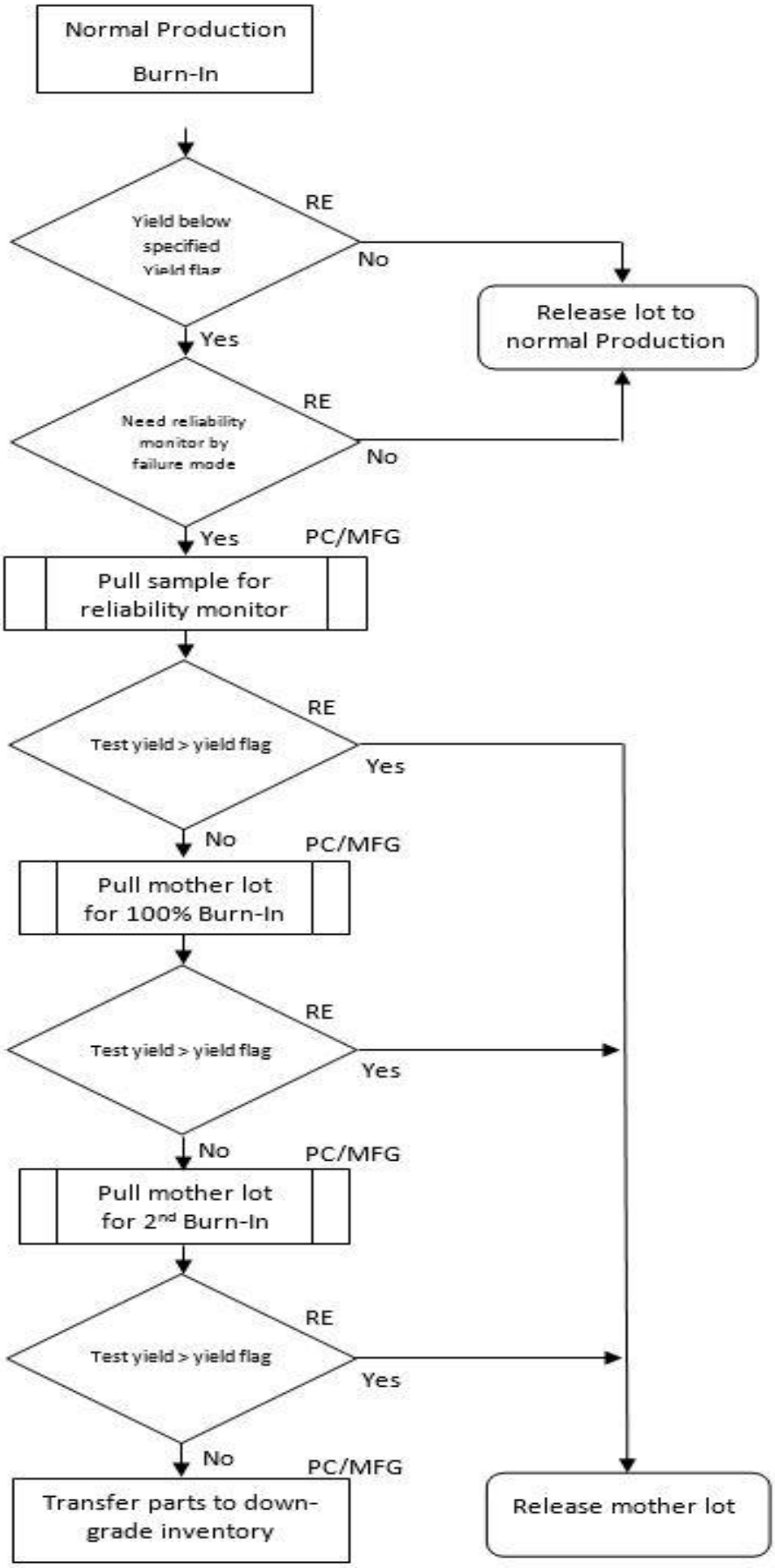

Figure 1 – Reliability Monitor Flow

2. Reliability Monitor Procedure

The Product Reliability Monitoring should be executed following below requirement (See below Table 1). All these topics cover the requirement from the spec of JESD 659 Failure-Mechanism-Driven Reliability Monitoring/ section 6.

	Item	Requirement
1	Test condition	HTOL, 168h, 125C, dynamic operating with Vcc-max, sample size:315ea
2	Monitoring frequency	Cover major foundry technology family in at least 1 year. Follow customer's spec if customer have special request.
3	Selection rule	1. Per each foundry/ process technology family. ISSI need to select one product for monitoring at least. 2. The product which has the largest quantity of finished goods in inventory would be preferred.
4	Reliability Monitoring Plan	RE should give a product monitoring plan annually for the folling whole year, and report it in "Quarterly Management Review Meeting f" for getting GM's approval
5	Reliability Monitoring Report	RE should publish the product monitoring report quarterly and report it in "Quarterly Management Review Meeting".

Table 1 : Product Reliability Monitoring Requirement Table

ISSI Reliability Test conditions

1. Device Related Tests

1.1 High Temperature Operating Life Test

Condition : Dynamic operation, T = 125 ℃.

Duration : Up to 1000 hrs, failed device were counted at 168, 500 and 1000hrs

Failures : When a device fails to pass production test program

Calculation : Both temperature and voltage acceleration factors are considered for the failure rate calculation; Poisson probability distribution with confidence level = 60% is assumed.

1.2 Infant Mortality Test

Condition : Dynamic operation, T=125 ℃

Duration : Up to 96 hrs, failed device were counted at 8, 16, 24 and 96 hrs

Failures : When a device fails to pass production test program

Calculation : Both temperature and voltage acceleration factors are considered for the failure rate calculation; Poisson probability distribution with confidence level = 60% is assumed

1.3 Electrostatic Discharge (ESD) and Latch-up Tests

ISSI currently performs three types of ESD tests :

1) The Human Body model (HBM), according to ANSI/ESDA/JEDEC JS-001
2) The Charge Device model (CDM), according to ANSI/ESDA/JEDEC JS-002

During the tests, the applied voltage is increased in steps until reaching the maximum passing voltage.

The test sequence for ESD is listed as following:

1) Zap all IO pins (+/-) respectively to V_{DD} and Vss pins.
2) Zap all IO pins (+/-) respectively to all other IO pins.
3) Zap all V_{DD} pins (+/-) respectively to all Vss pins.
4) Zap all V_{DD} pins (+/-) respectively to all other Vdd pins.

Latch-up test: In accordance with JEDEC standard No.78, the currents are injected into the input, output and I/O pins, and I_{cc} is monitored to see whether latch-up has occurred.

The test sequence of latch-up is listed as following:

1) Current trigger to all IO pins (+/-) respectively with all input pins biased during V_{DD} power is applied.
2) Voltage trigger to all V_{DD} pins respectively with all input pins biased during V_{DD} power is applied.

1.4 Soft Error Rate

(JEDEC Standard 89)

Source : Americium 241, with half life = 432.7 ± 0.5 years

Alpha particle activity: 4.948K Bq[1]

Alpha particle flux density: 4.53×10^5 / cm^2-hour

Acceleration factor: source α-intensity / package α-intensity.

Example: for molding compound with an emission of 0.001/cm^2-hr, the acceleration factor = 4.53×10^8,

[1] Bq abbreviates for becquerel, a unit to measure the radioactive strength [1 Bq= 30 alphas/min (2 pi emission rate)]; it names after the French physicist, Antoine-Henri Becquerel (1852-1908) who won the Nobel prize in Physics with Pierre and Marie Curie in 1903.

Test condition: After de-capsulation, the radioactive source was directly placed over the die surface. Both the source and die were covered to avoid ambient light; Pattern is written into the cell and data are continuously read out. The test arrangement is shown in below Figure 2~4.

Figure 2 – Radioactive Source: Americium 241

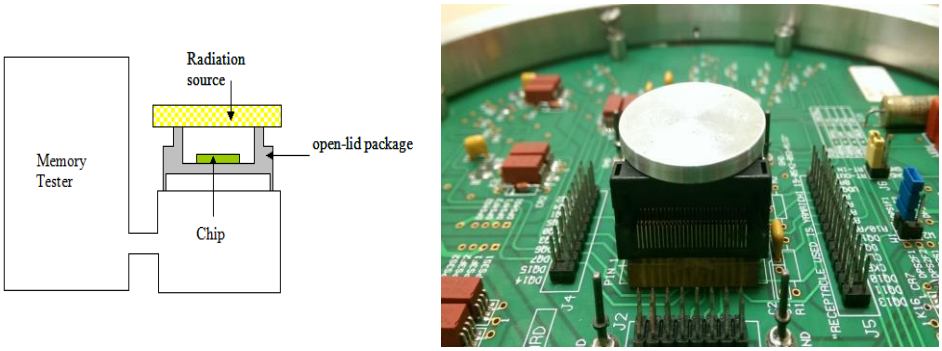

Figure 3 – SER Test Arrangement

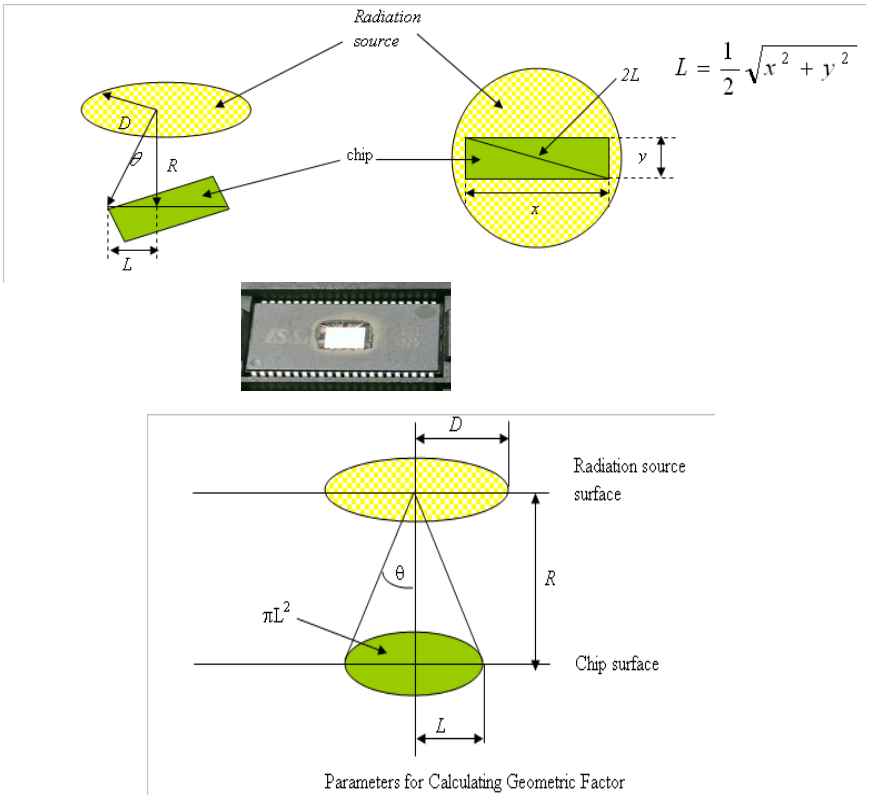

Figure 4 – Geometric Factor about how Alpha from Am source into chip surface

Endurance Cycling and Data Retention tests

(Refer to MIL-STD-883 1033 and JEDEC 22 A117)

ISSI currently performs these two special tests on Flash devices for reliability evaluation.

Endurance Cycling test evaluates the quality of the tunnel oxide of Flash products.

Condition : Continued program-erase operation to cause charge trapping or even breakdown in the tunnel oxide.

Duration : 100K cycles at room temperature and high temperature.

Failures : measure threshold shift or cell current that eventually cause failure of a cell to retain data

Calculation : percentage of cells that cannot retain data as a function of program-erase cycling

Data retention test measures the stability of electron in the floating gate of Flash products.

Condition : high temperature(typically, 125 or 150 ℃) with no bias

Duration : 1000 hours

Failures : measure threshold shift or cell current that eventually cause failure of a cell to retain data

Calculation : percentage of cells that cannot retain data after baking

2. Package Related Tests

2.1 Pre-condition Test

Procedure:

1) baking 24 hrs at 125 ℃;
2) moisture soaking at certain temperature and humidity level. For level 3: T=30 ℃ and RH=60%, for 192 hrs;
3) re-flowing solder IR at 240 ℃/260 ℃ for regular and Pb-free packages respectively

2.2 Highly Accelerated Stress Test

Condition : Steady-state temperature humidity bias, voltage is normally set at 1.1× Vcc, T = 130 ℃, 85% RH, 33.3 psi.

Duration: Electrical tests conducted at 96 hrs

(or 110℃/85%RH/264 hrs)

Failure: When device fails to pass production test program

Calculation : Both temperature and humidity acceleration factors are considered for the failure rate calculation. Poisson probability distribution with confidence level = 60% is assumed.

2.3 Temperature Cycling Test

Condition: T = -65 to +150 ℃ temperature cycle, transition period: 5 min.

Duration: Electrical tests conducted after 250 temperature cycles.

Failure: When device fails to pass production test program

Calculation: Poisson probability distribution with confidence level = 60% is assumed.

2.4 Pressure Cooker Test

Condition : No bias, T=121 ℃, relative humidity (RH) = 100%, pressure 15 psi.

Duration : Electrical tests conducted at 168 hrs for Non BGA pkg and 96hrs for BGA pkg. (Reference only for BGA)

Failure : When device fails to pass production test program

Calculation : Poisson probability distribution with confidence level = 60% is assumed.